## CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A system, comprising:

a plurality of nodes, wherein each node includes an active device and a memory subsystem coupled to the active device;

wherein an active device included in a node of the plurality of nodes includes a memory management unit configured to receive a virtual address generated within that active device and to responsively output a global address identifying a coherency unit, wherein a portion of the global address identifies a translation function;

wherein a memory subsystem included in the node is configured to perform the translation function identified by the portion of the global address on an additional portion of the global address in order to obtain a local physical address of the coherency unit;

wherein each active device included in the node is configured to use the portion of the global address identifying the translation function when determining whether a local copy of the coherency unit is currently stored in a cache associated with that active device;

wherein a home memory subsystem included in a home node of the plurality of nodes for the coherency unit is configured to store the portion of the global address identifying the translation function for the node, wherein active devices included in the home node are configured to generate a different value of the portion of the global address, wherein the different

value identifies a different translation function associated with the coherency unit in the home node; and

wherein if the home memory subsystem determines that the coherency transaction involving the coherency unit cannot be completed within the home node, the home memory subsystem is configured to provide the portion of the global address identifying the translation function for the node a home interface included in the home node for conveyance to the node.

2. (Original) The system of claim 1, wherein at least one bit included in the global address indicates whether the coherency unit identified by the global address is replicable in more than one of the plurality of nodes.

3. (Original) The system of claim 2, wherein if the at least one bit included in a different global address indicates that the different global address is not replicable in more than one of the plurality of nodes, the portion of the different global address includes additional address bits instead of identifying a translation function.

4. (Original) The system of claim 1, wherein the additional portion of the global address for the coherency unit generated by each active device in the plurality of nodes has a same value, and wherein active devices in different nodes of the plurality of nodes generate different values of the portion of the global address identifying the translation function.

5-6. ( Cancelled)

7. (Original) The system of claim 1, wherein the active device included in the node is configured to output the global address in an address packet on an address network coupling the active device to an additional active device within the node in order to initiate a coherency transaction for a coherency unit identified by the global address.

8. (Original) The system of claim 1, wherein a memory controller included in the memory subsystem is integrated in a same integrated circuit as the active device.

9. (Currently Amended) A method for use in a system comprising a plurality of nodes, wherein each node includes an active device and a memory subsystem coupled to the active device, the method comprising:

an active device included in a node of the plurality of nodes translating a virtual address generated within the active device to a global address identifying a coherency unit, wherein a portion of the global address identifies a translation function;

a memory subsystem included in the node performing the translation function identified by the portion of the global address on an additional portion of the global address in order to obtain a local physical address of the coherency unit;

an additional active device included in the node using the portion of the global address identifying the translation function when determining whether a local copy of the data is currently stored in a cache associated with the additional active device;

wherein at least one bit included in the global address indicates whether the coherency unit identified by the global address is replicable in more than one of the plurality of nodes; and

the active device translating a different virtual address to a different global address, wherein the at least one bit included in the different global address indicates that the different global address is not replicable in more than one of the plurality of nodes, and wherein the portion of the different

global address includes additional address bits instead of identifying a translation function.

10-11. (Cancelled)

12. (Original) The method of claim 9, further comprising active devices in different ones of the plurality of nodes generating a same value of the additional portion of the global address for the coherency unit, and active devices in different ones of the plurality of nodes generate different values of the portion of the global address identifying the translation function.

13. (Original) The method of claim 9, further comprising a home memory subsystem included in a home node of the plurality of nodes for the coherency unit storing the portion of the global address identifying the translation function for the node, wherein active devices included in the home node generate a different value of the portion of the global address, wherein the different value identifies a different translation function associated with the coherency unit in the home node.

14. (Original) The method of claim 13, wherein if the home memory subsystem determines that the coherency transaction involving the coherency unit cannot be completed within the home node, the home memory subsystem provides the portion of the global address identifying the translation function for the node a home interface included in the home node for conveyance to the node.

15. (Original) The method of claim 9, further comprising the active device included in the node outputting the global address in an address packet on an address network coupling the active device to an additional active device within the node in order to initiate a coherency transaction for a coherency unit identified by the global address.

16. (Original) The method of claim 9, further comprising an operating system executing on the active device creating a translation lookaside buffer entry corresponding

to the virtual address, wherein the translation lookaside buffer entry includes the global address, wherein the operating system selects the translation function in order to map the virtual address to the local physical address within a non-replicated range of local physical addresses of the memory subsystem.

17. (Original) The method of claim 16, further comprising the operating system executing on the active device in one of the nodes creating the translation lookaside buffer entry corresponding to the virtual address in response to deciding to replicate the coherency unit to the node from an additional one of the plurality of nodes.

18. (New) A method for use in a system comprising a plurality of nodes, wherein each node includes an active device and a memory subsystem coupled to the active device, the method comprising:

an active device included in a node of the plurality of nodes translating a virtual address generated within the active device to a global address identifying a coherency unit, wherein a portion of the global address identifies a translation function;

a memory subsystem included in the node performing the translation function identified by the portion of the global address on an additional portion of the global address in order to obtain a local physical address of the coherency unit;

an additional active device included in the node using the portion of the global address identifying the translation function when determining whether a local copy of the data is currently stored in a cache associated with the additional active device; and

an operating system executing on the active device creating a translation lookaside buffer entry corresponding to the virtual address, wherein the

translation lookaside buffer entry includes the global address, wherein the operating system selects the translation function in order to map the virtual address to the local physical address within a non-replicated range of local physical addresses of the memory subsystem.

19. (New) The method of claim 18, further comprising the operating system executing on the active device in one of the nodes creating the translation lookaside buffer entry corresponding to the virtual address in response to deciding to replicate the coherency unit to the node from an additional one of the plurality of nodes.